

What is claimed is:

1. A semiconductor memory device comprising:
a device substrate having a semiconductor layer
5 separated by a dielectric layer from a base substrate;
a memory cell array having a plurality of memory cells
formed and arranged on said semiconductor layer of said device
substrate, each said memory cell having a MOS transistor
structure with a body in an electrically floating state to
10 store data based on a majority carrier accumulation state of
said body; and
a sense amplifier circuit configured to perform data
read out of said memory cell array, said sense amplifier
circuit including a bipolar transistor for performing current
15 amplification of a memory cell selected during data reading.

2. The semiconductor memory device according to claim 1,
wherein

- said sense amplifier circuit has a pre-sense amplifier
20 including said bipolar transistor and a main sense amplifier
for amplification of an output of said pre-sense amplifier.

3. The semiconductor memory device according to claim 2,
wherein

- 25 said bipolar transistor of said pre-sense amplifier is a
lateral transistor formed on said semiconductor layer of said
device substrate, said lateral transistor having a collector
coupled to ground, a base connected to a drain of a
corresponding memory cell, and an emitter connected to said
30 main sense amplifier.

4. The semiconductor memory device according to claim 3,
wherein

- 35 said lateral transistor has its characteristics that a
current amplification factor increases with an increase in
base current within an operating current range during reading.

5. The semiconductor memory device according to claim 3,
wherein

5 said pre-sense amplifier has a first transfer gate for
connecting between the base of said lateral transistor and
the drain of the corresponding memory cell during reading,
and a second transfer gate for transferring write data to the
drain of the corresponding memory cell without through said
lateral transistor during writing.

10

6. The semiconductor memory device according to claim 5,
wherein

said first and second transfer gates are MOS transistors.

15 7. The semiconductor memory device according to claim 2,
further comprising:

amplifier and said memory cell array for selecting one from
among a plurality of bit lines of said memory cell array and
20 for connecting a selected bit line to said pre-sense
amplifier.

8. The semiconductor memory device according to claim 2,
wherein

25 said main sense amplifier has:

an operational amplifier having a one input terminal for
use as a sense node with cell data transferred thereto and a
remaining input terminal as a reference node with a data
sensing reference voltage given thereto;

30 a first current source load connected to said sense
node;

a first reference voltage generation circuit arranged to
include a second current source load connected to said
reference node, for generating said data sensing reference
35 voltage; and

a clamp circuit for clamping during reading a voltage of

a bit line of said memory cell array being connected to said sense node.

9. The semiconductor memory device according to claim 8,
5 wherein

said main sense amplifier further has a data latch connected to an output terminal of said operational amplifier for holding read data.

10 10. The semiconductor memory device according to claim
9, wherein

said data latch is used to temporarily hold write data therein.

15 11. The semiconductor memory device according to claim
8, wherein

said clamp circuit has:

a clamping MOS transistor interposed between said sense node and the bit line of said memory cell array;

20 an operational amplifier having a one input terminal to which a source voltage of said clamping MOS transistor is fed back and input and a remaining input terminal to which a clamp-use reference voltage is input, for driving by its output a gate of said clamping MOS transistor; and

25 a second reference voltage generation circuit for generating said clamp-use reference voltage.

12. The semiconductor memory device according to claim
11, wherein

30 said second reference voltage generation circuit comprises a diode whose cathode receives a read voltage to be given to the drain of a memory cell during reading and a current source load connected to an anode of said diode, and generates a clamp-use reference voltage substantially equal 35 in potential to said read voltage plus a forward voltage drop of said diode as added thereto.

13. The semiconductor memory device according to claim
8, wherein

5 said first reference voltage generation circuit
comprises:

two reference memory cells with data "0" and "1" being
written thereinto, respectively; and

10 two reference pre-sense amplifiers disposed between said
reference memory cells and said reference node for performing
current amplification of said reference memory cells,
respectively; and

two reference clamp circuits disposed between said
reference memory cells and said reference pre-sense
amplifiers, respectively, and wherein

15 said second current source load has two times as high
drivability as that of said first current source load.

14. The semiconductor memory device according to claim
1, further comprising:

20 a word-line driver arranged by using a bipolar
transistor, for driving a word line connected to the gate of
a memory cell in said memory cell array.

15. The semiconductor memory device according to claim
25 14, wherein

said word-line driver has a pull-up lateral transistor
and a pull-down lateral transistor which are formed at said
semiconductor layer of said device substrate.

30 16. The semiconductor memory device according to claim
15, wherein

said word-line driver further comprises:

a P-channel MOS ("PMOS") transistor interposed between a
collector and a base of said pull-up lateral transistor; and

35 an N-channel MOS ("NMOS") transistor interposed between
a collector and a base of said pull-down lateral transistor

and having a gate commonly coupled to a gate of said PMOS transistor.